



Parsa Mirfasihi

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I. Research Interests

Hardware Security; Secure Integrated Circuit (IC) Design; In-Memory Computing; Trustworthy AI Hardware; Photonic Computing and Co-Packaged Optics (CPO) for Space Applications.

II. Education

Ph.D. Student in Electrical and Computer Engineering
School of Electrical, Computing, and Software Engineering
University of Arizona (UofA), Tucson, AZ

August 2026–Present

Advisor: Soheil Salehi, Ph.D.

M.S. in Electrical and Computer Engineering
School of Electrical and Computer Engineering
San Francisco State University (SFSU), San Francisco, CA
Thesis: Machine-Learning-Enabled Interconnect Modeling for Timing Analysis of Advanced Integrated Circuits
GPA: 4.00/4.00

January 2024 – May 2026

Advisor: Hamid Mahmoodi, Ph.D.

B.S. in Electrical and Computer Engineering
School of Electrical and Computer Engineering
Iran University of Science and Technology (IUST), Tehran, Iran
Thesis: Design and Implementation of a Real-Time Object Detection and Classification System Using Deep Convolutional Neural Networks for Autonomous Vehicles
GPA: 3.70/4.00

September 2017 – May 2022

Advisor: Shahriar Baradaran Shokouhi, Ph.D.

III. Professional Experience

A. Industry Experience

Industrial Assessment Center (IAC)
Energy Engineer

September 2024 – April 2025

San Francisco State University, San Francisco, CA

Part-time, on-campus employment at San Francisco State University's Industrial Assessment Center, a program funded by the U.S. Department of Energy (DOE) through its Office of Energy Efficiency and Renewable Energy (EERE).

- Co-led on-site energy assessments of industrial and manufacturing facilities, identifying opportunities to improve energy efficiency and reduce operating costs.
- Analyzed facility energy consumption, electrical loads, and utility rate structures to evaluate energy use and identify cost-saving opportunities.
- Evaluated energy conservation measures through engineering calculations and economic analysis to assess technical feasibility and financial benefits.
- Prepared technical assessment reports documenting findings, supporting calculations, and recommendations for industrial efficiency improvements.

B. Research Experience

Power-Efficient, Resilient, Intelligent, and Secure Microsystems (PRISM) Lab

August 2026 – Present

Graduate Research Assistant (GRA)

University of Arizona, Tucson, AZ

School of Electrical, Computing, and Software Engineering

Advisor: Soheil Salehi, Ph.D.

- Investigate large language models (LLMs) and agentic AI for hardware design and security, including RTL obfuscation for intellectual property protection and post-synthesis validation of fault-hardening mechanisms.
- Contribute to power side-channel analysis and mitigation for FPGA and edge AI systems, including correlation-based cryptographic key recovery from convolutional neural network outputs.
- Investigate standard-cell analysis methods for hardware Trojan detection and mitigation to assess malicious modifications in integrated circuits.
- Develop evidence-grounded, LLM-assisted security assessment methods across printed circuit board design artifacts and examine security exposures and assurance evidence throughout the PCB assembly lifecycle.

Nano-Electronics & Computing Research Lab (NECRL)

January 2025 – July 2026

Graduate Research Assistant (GRA)

San Francisco State University, San Francisco, CA

School of Electrical and Computer Engineering

Advisor: Hamid Mahmoodi, Ph.D.

- Developed machine-learning-enabled interconnect modeling methods to improve the accuracy and efficiency of timing analysis for advanced semiconductor design.
- Conducted simulation-based validation of interconnect models to assess timing prediction accuracy and support reliable performance evaluation of integrated circuits.
- Developed automated analysis workflows to address interconnect challenges arising from technology scaling and support electronic design automation for advanced computing hardware.

C. Teaching and Mentoring Experience

Graduate Teaching Assistant (GTA)/Grader

August 2024 – December 2025

School of Electrical and Computer Engineering

San Francisco State University, San Francisco, CA

- Supported undergraduate engineering instruction across Digital Design/Lab (ENGR-356/357), Introduction to Microcontrollers (ENGR-294), Computer Systems (ENGR-456), Linear Systems Analysis (ENGR-305), Communication Systems (ENGR-449), Control Systems (ENGR-447), and Operational Amplifier Design (ENGR-442).
- Guided students in applying theoretical concepts to engineering problems, emphasizing analytical reasoning, systematic problem solving, and interpretation of results.
- Assisted students with coursework and laboratory assignments, helping them troubleshoot technical challenges and connect classroom concepts with practical implementation.
- Provided constructive feedback on student work to address conceptual misunderstandings and strengthen technical explanations and independent learning.

IV. Publications

A. Journal Manuscripts Under Review

1 journal manuscript under review

1. S. Ghimire, **P. Mirfasihi**, M. A. Chowdhury, H. K. Dharavath, et al., “Large Language Models and Attention-Based AI for Hardware Design and Security: Progress, Challenges, and Opportunities,” submitted to *Proceedings of the IEEE*, 2026. **Under review.** Preprint DOI: [10.48550/arXiv.2504.08854](https://doi.org/10.48550/arXiv.2504.08854).

B. Conference Publications and Submissions

7 manuscripts: 3 published, 3 accepted for publication, and 1 submitted

1. S. Ghimire, **P. Mirfasihi**, M. A. Chowdhury, V. Pugazhenth, H. K. Dharavath, et al., “Can Agents Secure Hardware? Evaluating Agentic LLM-Driven Obfuscation for IP Protection,” in *Proc. IEEE 44th VLSI Test Symposium (VTS)*, pp. 1–5, 2026. DOI: [10.1109/VTS69484.2026.11563377](https://doi.org/10.1109/VTS69484.2026.11563377).
2. **P. Mirfasihi**, A. Kim, H. Ramesh, J. Dean, M. Akbarsharifi, R. Akbarsharifi, et al., “FedLLM4HW: Carbon-Aware Federated Triage of Hardware Weaknesses in LLM-Generated Verilog Code,” in *Proc. 16th ACM International Green and Sustainable Computing Conference (IGSC)*, pp. 143–148, 2026. DOI: [10.1145/3797248.3816055](https://doi.org/10.1145/3797248.3816055).
3. V. Pugazhenth, M. M. A. Chowdhury, S. Ghimire, H. K. Dharavath, **P. Mirfasihi**, et al., “LeakSEAL: Power Side-Channel Leakage Analysis and Mitigation for Secure Edge AI Learning,” in *Proc. Great Lakes Symposium on VLSI*

(GLSVLSI), pp. 135–140, 2026. DOI: [10.1145/3787109.3816388](https://doi.org/10.1145/3787109.3816388).

4. **P. Mirfasihi**, S. Ghazali, X. Ramus, M. A. Chowdhury, S. Ghimire, P. Satam, and S. Salehi, “PCB-SAGE: LLM-Assisted Security Assessment with Grounded Evidence Across PCB Artifacts,” *IEEE International Conference on Physical Assurance and Inspection of Electronics (PAINE)*, 2026. **Accepted for publication.**
5. H. Gibbs, M. M. A. Chowdhury, V. Pugazhenth, **P. Mirfasihi**, S. Ghimire, X. Ramus, S. Shao, R. Yasaei, P. Satam, and S. Salehi, “LEAKI-PLC: Live End-to-End AES Key Recovery from Industrial PLCs via Electromagnetic Side-Channel Analysis,” *IEEE International Conference on Physical Assurance and Inspection of Electronics (PAINE)*, 2026. **Accepted for publication.**
6. A. Abolhasani Zeraatkar, P. Shabani Kamran, **P. Mirfasihi**, S. Khalaj Monfared, and H. Al-Asaad, “Power, Performance, and Area of HPC-Based Malware Detectors: An FPGA and Open-PDK ASIC Study,” *IEEE 17th Annual Information Technology, Electronics and Mobile Communication Conference (IEMCON)*, 2026. **Accepted for publication.** Preprint DOI: [10.48550/arXiv.2610.12795](https://doi.org/10.48550/arXiv.2610.12795).
7. **P. Mirfasihi**, J. V. Mandaliya, A. Shebaita, H. Mahmoodi, and S. Salehi, “DPiX: Closed-Form Five-Moment Extraction of a Double-Pi RC Load for Gate-Delay Estimation,” **Submitted** to the *Design, Automation and Test in Europe Conference (DATE 2027)*.

C. Book Chapters in Preparation

1. S. Ghimire, **P. Mirfasihi**, M. A. Chowdhury, V. Pugazhenth, H. K. Dharavath, K. I. Gubbi, N. Tarighat, H. Homayoun, R. Yasaei, P. Satam, and S. Salehi, “Hardware Design Leveraging LLMs: From IP to SoC,” Chapter 3. **In preparation.**

V. Selected Funding Proposal Development

National Science Foundation (NSF), RET: Assisted in preparing the proposal titled “*RET Site: Community College Research Experiences in Trustworthy AI-Assisted Chip Design.*”

National Science Foundation (NSF), SHF: FET: Assisted in preparing the proposal titled “*Collaborative Research: SHF: FET: Algorithm-Hardware Co-Design for Trustworthy and Energy-Efficient Edge AI Leveraging Post-CMOS Devices.*”

National Science Foundation (NSF), CAREER: Assisted in preparing a proposal on reliable and secure compute-in-memory architectures for edge AI in extreme environments, leveraging voltage-gated spin-orbit torque MRAM and hardware–algorithm co-design.

VI. Honors and Awards

A. Awards and Scholarships

Herbold One Fellowship

August 2026

School of Electrical, Computing, and Software Engineering, University of Arizona
Fellowship Award Amount: **\$69,590**

Outstanding Graduate Distinguished Achievement Award

May 2026

School of Electrical and Computer Engineering, San Francisco State University

[View Certificate](#)

Graduate Student Honoree, Department of Electrical and Computer Engineering

May 2026

School of Electrical and Computer Engineering, San Francisco State University

1st Place in Both Best Overall Design and Upper Division

May 2026

AI Hardware Design League (AI-HDL)

Led and competed as a member of the San Francisco State University team, earning top honors in both categories at this worldwide hardware design competition.

[View University Announcement](#)

3rd Place Overall**December 2025***San Francisco State University Fall 2025 Project Showcase**Recognized with third place overall among all participants for the research poster titled “Machine-Learning-Enabled Interconnect Modeling for Timing Analysis of Advanced Integrated Circuits.”***B. Travel Grants****Student Travel Grant****April 2026***Design Automation Conference (DAC 2026)**Awarded by: Department of Electrical and Computer Engineering**Award Amount: \$1,500***VII. Leadership and Professional Service****Speaker & Pioneer Relations Chair****October 2026***Iranian American Pioneers (IAP) Summit**Organizing Committee Member (Volunteer)*[View Official Committee Listing](#)**Selected as Co-Lead Mentor and Co-Organizer****January 2027***AI Hardware Design League (AI-HDL 2027)***Selected as Co-Organizer and Lead Mentor****November 2026 – May 2027***GhostGate Hardware Hacking Competition, IEEE HOST 2027***VIII. Peer Review and Professional Service****A. Technical Paper Reviewing**

- Reviewed **three** conference manuscripts for *PAINE* as a Sub-Reviewer, July 2026.
- Served as a **Sub-Reviewer** for the *8th Workshop on Top Picks in Hardware and Embedded Security*, co-located with ICCAD 2026, evaluating **four** nominated research papers, October 2026.
- Reviewed **two** survey manuscripts for *ACM Computing Surveys (CSUR)* as a Sub-Reviewer, September 2026.

IX. Training and Certifications

- **Verilog HDL: VLSI Hardware Design Comprehensive Masterclass**, Udemy
- **Teradyne J750 Automated Test Equipment Training and Volunteer Service** [View Certificate](#)
San Francisco State University, NECRL Lab
Selected as the sole student volunteer for Summer 2025. Completed hands-on training with a Teradyne professional in J750 calibration and operation, and performed integrated circuit testing on chips designed by students and alumni.

X. Professional Skills

- **Design & Verification** – Digital and mixed-signal IC design, ASIC/FPGA and SoC design, RTL design and verification, static timing analysis, low-power design, and design for test (DFT).
- **Physical Design & EDA** – RTL-to-GDSII implementation, placement and routing, parasitic extraction, timing closure, and optimization using Synopsys Design Compiler, PrimeTime, and VCS; Cadence Virtuoso, Innovus, and Genus.
- **Programming & Automation** – Python, C/C++, SystemVerilog, Tcl, Linux/Unix scripting, and machine learning for electronic design automation.
- **Hardware & Measurement** – Teradyne J750 automated test equipment, oscilloscopes, logic analyzers.

XI. Professional Affiliations and Memberships

- **Institute of Electrical and Electronics Engineers (IEEE) Student Member** **January 2026 – Present**

XII. Leadership and Community Service

- **Volunteer**, IEEE VLSI Test Symposium (VTS) **April 2026**
Supported conference operations and facilitated event activities, serving the engineering research community and contributing to the smooth delivery of the symposium.
- **President**, Iranian Student Association Center **August 2025 – May 2026**
San Francisco State University
Represented and supported the Iranian student community at San Francisco State University through service as association president.

XIII. Graduate Courses Completed

ENGR 848: Digital VLSI Design <i>San Francisco State University</i>	Spring 2025
CSC 842: Human-Computer Interaction <i>San Francisco State University</i>	Spring 2025
ENGR 844: Embedded Systems <i>San Francisco State University</i>	Fall 2024
ENGR 852: Advanced Digital Design <i>San Francisco State University</i>	Fall 2024
ENGR 845: Neural-Machine Interfaces <i>San Francisco State University</i>	Spring 2024
ENGR 850: Digital Design Verification <i>San Francisco State University</i>	Spring 2024

XIV. References

Dr. Soheil Salehi

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